QUIZ-II on UNIT-II

Instructions:

Please mention registration Number, Name and date

Timing and marks details are written on each slide
Total no of questions = 30
Each question has a time limit which is displayed along with the question

29/12/2018

Computer Architecture & Organization

ALL THE BEST

1.What are the phases of instruction cycle ?(20 Sec)
Ans - Fetch , Decode & Execute.

2. One byte equals to how many bits (1min)

A. 4
B. 6
C. 8 - Ans
D. 10

3.Which F/F is set when IEN is 1 ? : __(*20sec)*

A. F - Ans
B. R
C. E
D. I

4. Where the result of an arithmetic and logical operation are stored in memory reference instructions ? (40 Sec)

A. TR
B. DR
C. AC - Ans
D. IR

5.Which of the following is not a memory reference instruction (30 sec)

A. 010
B. 111 - Ans
C. 101
D. 110

6. What is FGI ? (40sec)

A. *Flag Input Buffer*
B. *Input Flag - Ans*
C. Input device Flag
D. Flag for Input
E. All of the above

7. An exception condition in a computer system caused by an event external to the CPU is known as? (20sec)

A. Halt
B. Process
C. Interrupt - Ans
D. None of the above

8. IR (instruction register) has mainly how many fields ? ***(1 min)***

Ans – Direct / indirect addressing bit – optional ,Opcode ,address field

9.What is the instruction size of register reference instruction if the address field of IR is 16 bit long ? (40 sec)

A. 4
B. 8
C. 16 - Ans
D. 12

10. The decoded instruction is stored in _____**(30 sec)**

A. PC
B. AR
C. IR - Ans
D. DR

11. During fetch cycle which of the following transfer takes place ?(50 sec)

A. **AR ← PC**

B. **IR ← M[AR], PC ← PC + 1**

C. **AR ← IR(0~11), I ← IR(15)**

D. **D_0...D_7 ← Decode IR(12 ~ 14)**

E. **Both A & B - Ans**

F. **All of the above**

12. Which bit identifies the given instruction is memory reference or register reference or input output ? ____ (40sec)

A. D0
B. D2
C. D6
D. D7 **- Ans**

13. During decode cycle which of the following transfer takes place ?**(1 min)**

A. **AR ← PC**

B. IR ← M[AR], PC ← PC + 1

C. AR ← IR(0~11), I ← IR(15) - Ans

D. D_0...D_7 ← Decode IR(12 ~ 14) - Ans

E. Both A & B

F. All of the above

14. For a computer system of with the capacity of 16,384 words,40 bits per word , what will be size of IR ? (1 min)

A. 12

B. 16

C. 40 **- Ans**

D. 14

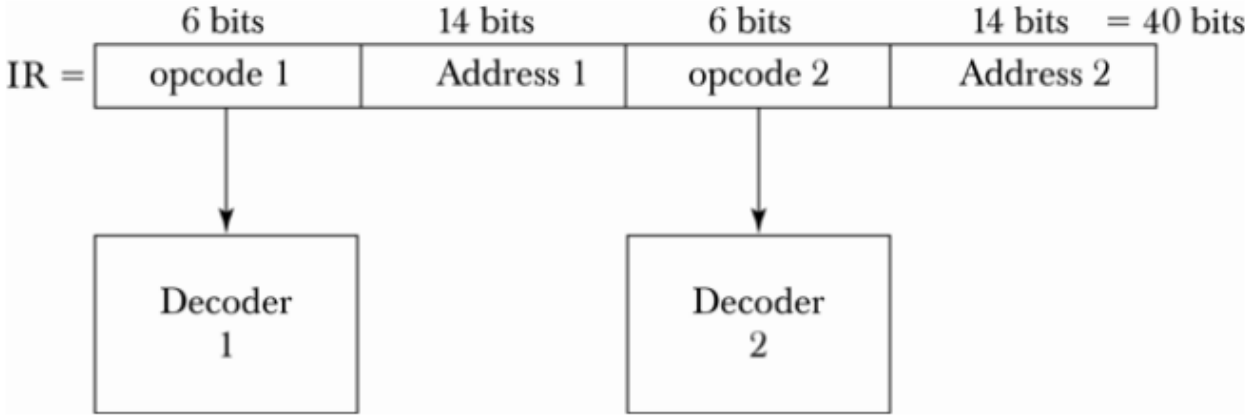
15. **For a computer system of with the capacity of 16,384 words,40 bits per word , what will be size of AR** (50sec)

A. 12
B. 16
C. 40
D. 14 **- Ans**

16. An output program resides in memory starting from address 2300.It is executed after the computer recognizes an interrupt when FGO becomes 1(while IEN = 1). What instruction must ve placed at address 1 ?(2min)

A. BUN 2300 **- Ans**
B. BUN 0
C. AR <- PC
D. PC <- PC + 1

17. **For a computer system of with the capacity of 16,384 words,40 bits per word , what will be size of IR. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no indirect mode bit).Two instructions are packed in one memory word, and a 40-bit instruction register IR is available in the control unit. Formulate a procedure for fetching and executing instructions for this computer.**
(3 min)



1. Read 40-bit double instruction from memory to IR and then increment PC.
2. Decode opcode 1.
3. Execute instruction 1 using address 1.
4. Decode opcode 2.
5. Execute instruction 2 using address 2.
6. Go back to step 1.

18.Write the instruction which will take place in T0 time . (1 min)

AR ← PC - Ans

19.Write the instruction which will take place in T1 time . (1 min)

IR ← M[AR], PC ← PC + 1 - Ans

20.Write the instruction which will take place in T2 time . (1 min)

AR ← IR(0~11), I ← IR(15) - Ans

D_0...D_7 ← Decode IR(12 ~ 14) - Ans

21. What is r = ? In register reference instruction ? (50 sec)

A. **$D_7 I'T_3$ - Ans**

B. $D_7 ' IT_3$

C. $D_7 IT_3 '$

D. $D_7 IT_3$

22. What is p = ? In input output instruction reference instruction ? (50sec)

A. D_7IT_3 - Ans

B. $D_7'IT_3$

C. D_7IT_3'

D. $D_7I'T_3$

23. What is the meaning of
AC(0-7) ← INPR, FGI ← 0 (1 min)
Ans – reading the input from the input device.

24.At the beginning (interrupt cycle)of the next instruction cycle, the instruction that is read from memory is in address _____ (50 sec)

A. 1 **- Ans**

B. 0

C. BUN

D. BSA

25. The instruction that returns the control to the original program ? (50 sec)

A. is "indirect BUN 0“ - Ans
B. is "indirect BUN 1“
C. is "indirect BUN 00“
D. is "indirect BSA 0"

26. Register Transfer Statements for Interrupt Cycle? (1min)

A. R F/F $\leftarrow$ 1 if IEN (FGI + FGO)$T_0'T_1'T_2$
B. R F/F $\leftarrow$ 1 if IEN (FGI + FGO)$T_0'T_1'T_2'$ - Ans
C. R F/F $\leftarrow$ 1 if IEN (FGI + FGO)$T_0'T_1T_2'$
D. R F/F $\leftarrow$ 1 if IEN (FGI + FGO)$T_0T_1T_2$

27. The interrupt cycle : What happens in T_0 (40 sec)

A. RT_0: AR ← 0, TR ← PC - Ans

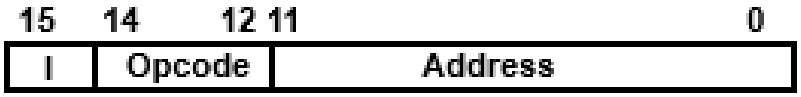
B. RT_0: AR ← 0, TR ← PC + 1

C. RT_0: AR ← 1, TR ← PC

D. RT_0: AR ← 0, DR ← PC

28. Draw the IR for Memory reference instruction ? (1 min)

Memory-Reference Instructions (OP-code = 000 ~ 110)

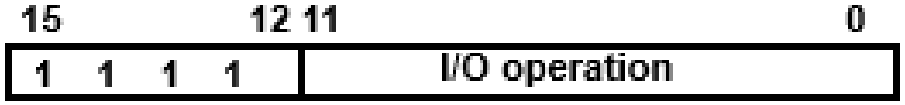


29. Draw the IR for Register reference instruction ? (1 min)

Register-Reference Instructions (OP-code = 111, I = 0)

30. Draw the IR for input output instruction (1 min)

Input-Output Instructions **(OP-code =111, I = 1)**



END OF QUIZ-II